

# **NEWS RELEASE**

For more information, contact:  
Larry Lapidés  
Vice President of Sales  
Imperas Software  
(925) 519-1234  
larryl@imperas.com  
<http://www.imperas.com>

## **ARM Cortex-A15 and Cortex-R4 Fast Processor Models Provided by Imperas and OVP**

*Open Source Models Available From Open Virtual Platforms*

**OXFORD, United Kingdom, October 25, 2012** – Imperas™, which is a member of the [ARM Connected Community](#), has released its models of the ARM® Cortex™-A15, Cortex™-R4, Cortex™-R4F and ARM1176™ processor cores. These models, as with all OVP models of the ARM processor cores, are now available from Open Virtual Platforms™ (OVP™). Support from OVP includes example virtual platforms incorporating the cores, with the processor core models also supported in Imperas' advanced software development tools. The models, together with the OVP and Imperas M\*SDK tools, will be demonstrated at the ARM TechCon conference October 31 and November 1 in Santa Clara.

The OVP Fast Processor Models and example platforms are available from the Open Virtual Platforms website, [www.OVPworld.org/ARM](http://www.OVPworld.org/ARM). The new models of the ARM processor cores, as well as models of the other ARM processors including the ARM7, ARM9, ARM10, ARM11 and Cortex-A, Cortex-R, and Cortex-M families, work with the Imperas and OVP simulators, and have shown exceptionally fast simulation performance of hundreds of millions of instructions per second. The OVP Fast Processor Models include support for both the 32 and 16-bit instructions, as well as the MMU, MPU, TCM, VFP, NEON, TrustZone, virtualization and Large Physical Address Extension (LPAE) features.

“The ARM Cortex-A15 and R4 processor cores are state of the art cores, with significant complexity in and of themselves, and even more complexity when considered in the context of the SoCs that implement these cores,” said Simon Davidmann, president and CEO, Imperas and founding director of the OVP initiative. “Software engineers using advanced cores demand additional tools for debug, test, analysis and optimization, and the OVP processor core models together with the Imperas M\*SDK tools provide the needed capabilities.”

All OVP processor models are instruction accurate, and very fast, focused on enabling embedded software developers, especially those building hardware-dependent software such as firmware and bare metal applications, to have a development environment available early to accelerate the software development cycle. OVP processor models employ a state of the art just-in-time code morphing engine to achieve the simulation speed. Virtual platforms utilizing these OVP processor models can be created with the OVP peripheral and platform models, or the processor models can be integrated into SystemC/TLM-2.0 based virtual platforms using the native TLM-2.0 interface available with all OVP models. The native TLM-2.0 interface enables multiple instantiations of the processor models in a single virtual platform, just as any other component would be instantiated. The OVP simulator can also be encapsulated within the Eclipse IDE, enabling easy use for software developers.

OVP also has reference virtual platforms incorporating the ARM cores, including a virtual platform of the ARM Versatile Express development board using any of the ARM Cortex-A family of models. These reference platforms are all available as source code, and are easily modified to add or change the memory and peripheral components to customize the platform as required for software development.

In addition to working with the OVP simulator OVPsim™, the OVP Fast Processor Models work with the Imperas Multiprocessor/Multicore/Multithread Software Development Kit (M\*SDK™). These advanced tools for multicore software verification and analysis include key tools for software development on virtual platforms such as OS and CPU-aware tracing (instruction, function, task, event), hot-spot profiling, code coverage and memory and cache analysis. The Verification, Analysis and Profiling (M\*VAP™) tools utilize the Imperas SlipStreamer™ patent pending binary interception technology. SlipStreamer enables these analytical tools to operate without any modification or instrumentation of the software source code, i.e., the tools are completely non-intrusive.

#### **Available OVP Fast Processor Models of ARM cores**

The following specific models are available from OVP:

ARM7TDMI, ARM720T, ARM7EJ-S

ARM920T, ARM922T, ARM926EJ-S, ARM940T, ARM946E, ARM966E-S, ARM968E-S

ARM1020E, ARM1022E, ARM1026EJ-S

ARM1136J-S, ARM1156T2-S, ARM1176JZ-S

Cortex-A5, Cortex-A8, Cortex-A9, Cortex-A15 (including MPCore versions as appropriate)

Cortex-M3, Cortex-M4, Cortex-M4F

Cortex-R4, Cortex-R4F

**About Imperas** ([www.Imperas.com](http://www.Imperas.com))

For more information about Imperas, please go to the Imperas [website](http://www.Imperas.com).

**About the Open Virtual Platforms Initiative** ([www.OVPworld.org](http://www.OVPworld.org))

For more information about OVP, please go to the About OVP page on the OVP [website](#).

Detailed quotations regarding OVP are available from <http://www.ovpworld.org/quotes>.

# # #

*Imperas, Open Virtual Platforms, OVP, OVPSim, M\*SDK, M\*VAP and SlipStreamer are trademarks of Imperas Software Limited. Imperas acknowledge trademarks or registered trademarks of other organizations for their respective products and services.*